

# STIC Search Report

# STIC Database Tracking Number: 190827

TO: Pinchus Laufer Location: RND 1C81

Art Unit: 2100

**Tuesday, May 23, 2006** 

Case Serial Number: 10/720030

From: Shirelle Green Location: EIC 2100

**RND 4B28** 

Phone: 272-3487

Shirelle.Green@uspto.gov

## Search Notes

Pinchus,

Attached are the results for your Litigation search for 6,324,639.

There were no cases found for this Patent Number...

If you have questions, please feel free to call.

Shirelle Green~Technical Information Specialist US Patent & Trademark Office STIC, EIC2100 Randolph 4B28 (Phone) 571-272-3487 (Fax) 571-273-0044



# **SEARCH REQUEST FORM**

## Scientific and Technical Information Center

Requester's Full Name: Pinchus Laufer		Examiner # : <b>73139</b> Date:	5/22/06		
Art Unit: 2100 Phone Number 272-3599		Serial Number: <u>10/720,030</u>			
Mail Box Location: 1C81	I	Results Format Preferred (circ	le): PAPER	DISK	E-MAIL
If more than one search is submitte				*****	****
Please provide a detailed statement of the sear elected species or structures, keywords, synon Define any terms that may have a special mea cover sheet, pertinent claims, and abstract.	yms, acronyms, and i	egistry numbers, and combine with	the concept or	utility of 1	the invention.
Title of Invention:					·
Inventors (please provide full names):			•		
			··-		
Earliest Priority Filing Date:		<del></del>			
*For Sequence Searches Only* Please include appropriate serial number.	all pertinent informa	tion (parent, child, divisional, or iss	ued patent num	bers) alonį	g with the
	Litiga 6,324,	,			
Inventor: Taketo Heishi et al		O.G. Date:	Feb 10,	2004	
**************************************					
STAFF USE ONLY	Type of Search		••		
Searcher: <u>Shirelle Green</u>	Sequence (#)	STN		<del></del>	
Searcher Phone #: <u>571-272-3487</u>	AA Sequence (#)	Dialog	<u> </u>		
Searcher Location: 4B28	Structure (#)	Questel/Orbit	8		
Date Searcher Picked Up: 5 3 00	Bibliographic	Dr.Link	- · · · · · - · · · · · · · · · · · · ·		
Date Completed: 5 23 0 6	Litigation	Lexis/Nexis			
Searcher Prep & Review Time:	Fulltext	Sequence Systems		·	
Clerical Prep Time:	Patent Family	WW-W/Internet			
Online Time:	Other	ther (specify)	Hund	2 Z	0.00

#### 1 of 1 DOCUMENT

#### UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT

#### 6324639

#### Link to Claims Section

November 27, 2001

Instruction converting apparatus using parallel execution code

INVENTOR: Heishi, Taketo - Osaka, Japan (JP); Tanaka, Tetsuya - Ibaraki, Japan (JP); Higaki, Nobuo - Osaka, Japan (JP); Takayama, Shuishi - Takarazuka, Japan (JP); Odani, Kensuke - Kyoto, Japan (JP)

APPL-NO: 280777 (09)

FILED-DATE: March 29, 1999

**GRANTED-DATE:** November 27, 2001

PRIORITY: March 30, 1998 - 10083368, Japan (JP); April 8, 1998 - 10095647, Japan (JP)

ASSIGNEE-PRE-ISSUE: April 26, 1999 - ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS)., MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD. 1006, OAZA KADOMA, KADOMA-SHIOSAKA-FU, (1), Reel and Frame Number: 009918/0083

ASSIGNEE-AT-ISSUE: Matsushita Electric Industrial Co., Ltd., Osaka, Japan (JP), Foreign company or corporation (03)

CORE TERMS: register, decoder, processor, buffer, stored, processing, node, format, dependency, bit ...

#### **ENGLISH-ABST:**

A processor can decode short instructions with a word length equal to one unit field and long instructions with a word length equal to two unit fields. An opcode of each kind of instruction is arranged into the first unit field assigned to the instruction. The number of instructions to be executed by the processor in parallel is s. When the ratio of short to long instructions is s-1:1, the s-1 short instructions are assigned to the first unit field to the s-1th unit field in the parallel execution code, and the long instruction is assigned to the sth unit field to the (s+k-1)th unit field in the same parallel execution code.

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Library: PATENTS

File: ALL

### **No Documents Found!**

No documents were found for your search terms "6324639 or 6,324,639"

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File: **JNLS** 

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Patent Search - Number: 6324639

No cases found.

Return to Search

(Charges for search still apply)

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```
us6324639/pn
 ** SS 1: Results 1
 Search statement
?prt full nonstop legalall
 1/1 PLUSPAT - (C) QUESTEL-ORBIT
 PN - US6324639 B1 20011127 [US6324639]
     - (B1) Instruction converting apparatus using parallel execution code
 PA - (B1) MATSUSHITA ELECTRIC IND CO LTD (US)
 PAO - Matsushita Electric Industrial Company, Ltd., Osaka [JP]
    - (B1) HEISHI TAKETO (JP); ODANI KENSUKE (JP); HIGAKI NOBUO (JP);
       TANAKA TETSUYA (JP); TAKAYAMA SHUISHI
 AΡ
     - US28077799 19990329
                             [1999US-0280777]
     - JP8336898 19980330
                            [1998JP-0083368]
      - JP9564798 19980408
                            [1998JP-0095647]
 IC - (B1) G06F-009/30 G06F-009/38 G06F-009/44
 ICAA- G06F-009/38 [2006-01 A - I R M EP]
 ICCA- G06F-009/38 [2006 C - I R M EP]
     - G06F-009/38E6
     - G06F-009/38F
 PCL - ORIGINAL (0): 712212000; CROSS-REFERENCE (X): 712023000 712206000
       712215000 712245000
 DT - Basic
 CT - US3955180; US4611281; US4858105; US5452461
 STG - (B1) U.S. Patent (no pre-grant pub.) after Jan. 2, 2001
     - A processor can decode short instructions with a word length equal to
       one unit field and long instructions with a word length equal to two
       unit fields. An opcode of each kind of instruction is arranged into
       the first unit field assigned to the instruction. The number of
       instructions to be executed by the processor in parallel is s. When
       the ratio of short to long instructions is s-1:1, the s-1 short
       instructions are assigned to the first unit field to the s-1th unit
       field in the parallel execution code, and the long instruction is
       assigned to the sth unit field to the (s+k-1)th unit field in the same
       parallel execution code.
 UP - 2001-49
 1/1 LGST - (C) EPO
 PN - US6324639 B1 20011127 [US6324639]
 AP - US28077799 19990329 [1999US-0280777]
 ACT - 20040210 US/RF-A
       REISSUE APPLICATION FILED
       EFFECTIVE DATE: 20031124
    - 2004-08
 1/1 CRXX - (C) CLAIMS/RRX
 PN - 6,324,639 A 20011127 [US6324639]
 PA - Matsushita Electric Industrial Co Ltd JP
 ACT - 20031124 REISSUE REOUESTED
       ISSUE DATE OF O.G.: 20040210
       REISSUE REQUEST NUMBER: 10/720030
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EXAMINATION GROUP RESPONSIBLE FOR REISSUEPROCESS: 2183

10/720030; Pinchus Laufer